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Nyfea product specification

PRODUCT SPECIFICATION

Customer : _____

Product Name : **Flip-Flop**

Part Number : **SN74LVC1G175**

Issue Date : _____

Prepared	Checked	Customer Check
ChenTT	Zelig	

NYFEA

SN74LVC1G175：Single D-Type Flip-Flop with Asynchronous Clear

DESCRIPTIONS

The SN74LVC1G175 single D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G175 device has an asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When $\overline{CLR}$ is low, Q is forced into the low state, regardless of the clock edge or data on D.

The SN74LVC1G175 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

This device available in Green SOT23-6 and SC70-6 packages. It operates over an ambient temperature range of -40°C to +125°C.

FEATURES

- **Operating Voltage Range: 1.65V to 5.5V**
- **Low Power Consumption: 0.1μA (TYP)**
- **Operating Temperature Range: -40°C to +125°C**
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at V_{CC}=3.0V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection**
- **Micro Size Packages: SOT23-6, SC70-6**

APPLICATIONS

- **Enterprise Switching**
- **Telecom Infrastructure**
- **Servers**
- **Medical Healthcare and Fitness**
- **PC/Notebook**
- **Motor Drives**

PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
SN74LVC1G175	SN74LVC1G175DCKR	-40°C ~+125°C	SC70-6 (4)	D65	MSL3	Tape and Reel,3000
	SN74LVC1G175DBVR	-40°C ~+125°C	SOT23-6	C755	MSL3	Tape and Reel,3000

NOTE:

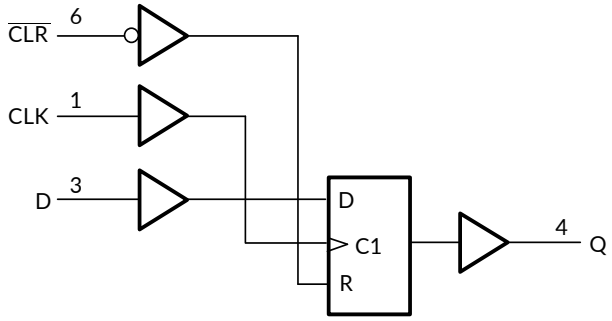
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) Equivalent to SOT363.

LOGIC DIAGRAM (POSITIVE LOGIC)



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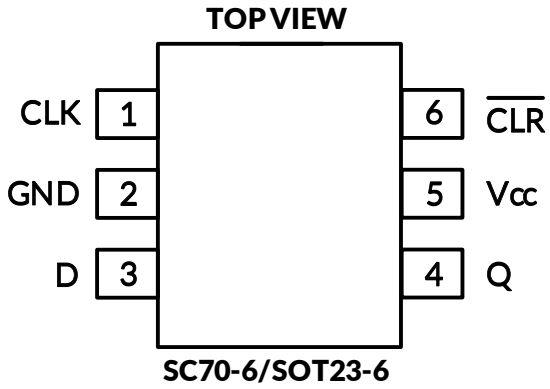
PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)



PIN	NAME	I/O	FUNCTION
1	CLK	I	Clock Input
2	GND	P	Ground
3	D	I	Input
4	Q	O	Output
5	V_{CC}	P	Power pin
6	$\overline{CLR}$	I	Clear Data Input

Function Table

INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_0
L	X	X	L

(1) H=High Voltage Level
L=Low Voltage Level
X=Don't Care

REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
Rev A.1	2026/01/13	Initial version completed

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA

Package Thermal Impedance

PARAMETER			MIN	MAX	UNIT
θ_{JA}	Package thermal impedance (4)	SOT23-6		230	°C/W
		SC70-6		265	

Temperature

PARAMETER		MIN	MAX	UNIT
Temperature	Junction temperature, T_J (5)	-65	150	°C
	Storage temperature, T_{stg}	-65	150	

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

	VALUE	UNIT
Human-Body Model (HBM)	±2000	V
Charged-Device Model (CDM)	±1000	
Machine Model (MM)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65	5.5	V
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.75 x V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7 x V_{CC}		
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V to 1.95V		0.25 x V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3 x V_{CC}	
Input Voltage	V_I		0	5.5	V
Output Voltage	V_O		0	V_{CC}	V
High-Level Output Current	I_{OH}	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
Low-Level Output Current	I_{OL}	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Input Transition Rise or Fall	Δt / Δv	V_{CC}=1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC}=3.3V ± 0.3V		10	
		V_{CC}=5V ± 0.5V		10	
Operating Temperature	T_A		-40	+125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	Data or Control Inputs	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1		μA
				Full			±5	
	I_{off}	V_I or V_O=5.5V	0	+25°C		±0.1		μA
				Full			±10	
	I_{CC}	V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1		μA
				Full			10	
	ΔI_{CC}	One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i (Input Capacitance)		V_I = V_{CC} or GND	3.3V	+25°C		5.5		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CC}=1.8V ± 0.15V		V_{CC}=2.5V ± 0.2V		V_{CC}=3.3V ± 0.3V		V_{CC}=5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}			-40°C to 85°C		30		65		100		155	MHz
			-40°C to 125°C						100		155	
t_w	CLK High or low		-40°C to 85°C	8		4		3		2		ns
			-40°C to 125°C					3		2		
	$\overline{CLR}$ low		-40°C to 85°C	12		5		3.4		2		
			-40°C to 125°C					3.4		2		
t_{su}	Data		-40°C to 85°C	10.4		4.6		3.2		2		ns
			-40°C to 125°C					3.2		2		
	$\overline{CLR}$ inactive		-40°C to 85°C	8.4		3.8		2.6		1.8		
			-40°C to 125°C					2.6		1.8		
t_h			-40°C to 85°C	0.5		0.5		0.5		0.5		ns
			-40°C to 125°C					0.5		0.5		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CC}=1.8V ± 0.15V		V_{CC}=2.5V ± 0.2V		V_{CC}=3.3V ± 0.3V		V_{CC}=5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			-40°C to 85°C	30		65		100		155		MHz
t_{pd}	CLK	Q	-40°C to 85°C	2.5	25.5	2	13	1.4	9.5	1	7	ns
	$\overline{CLR}$	Q	-40°C to 85°C	2.5	23	2	10	1.2	7.5	1	6	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CC}=1.8V ± 0.15V		V_{CC}=2.5V ± 0.2V		V_{CC}=3.3V ± 0.3V		V_{CC}=5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			-40°C to 85°C	30		65		100		155		MHz
			-40°C to 125°C					100		155		
t_{pd}	CLK	Q	-40°C to 85°C	2.7	27.5	2.2	14.1	1.6	11	1.5	8.2	ns
			-40°C to 125°C	2.7	28.3	2.2	15	1.6	11.5	1.5	9	
	$\overline{CLR}$	Q	-40°C to 85°C	2.7	24.5	2.2	11	1.5	9	1.3	7	
			-40°C to 125°C	2.7	25	2.2	12	1.5	9.5	1.3	7.5	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

Operating Characteristics

T_A = +25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power Dissipation Capacitance	f = 10 MHz	12	16	21	24	pF

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, unless otherwise noted.

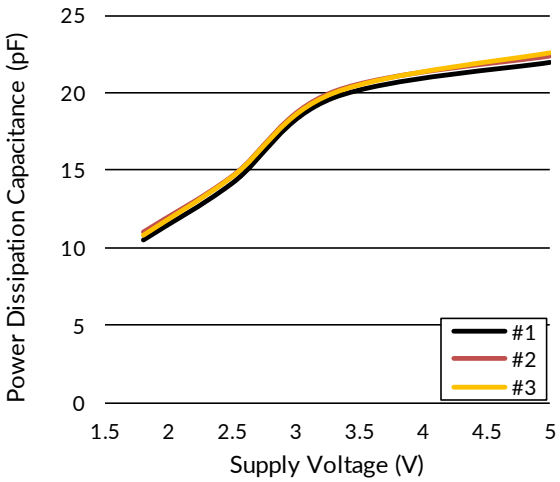
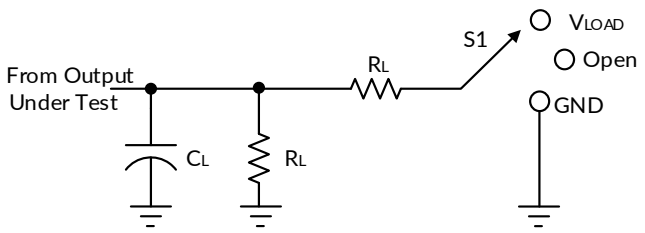


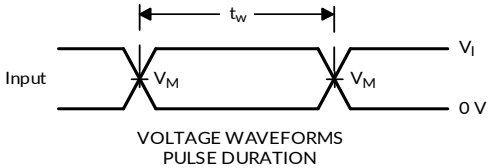
Figure 1. Voltage vs Capacitance

PARAMETER MEASUREMENT INFORMATION

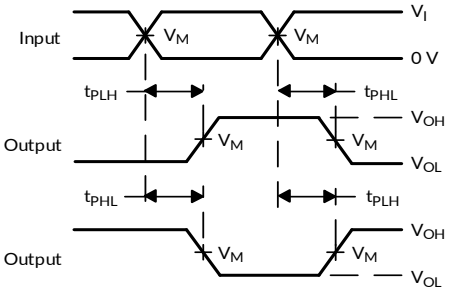


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

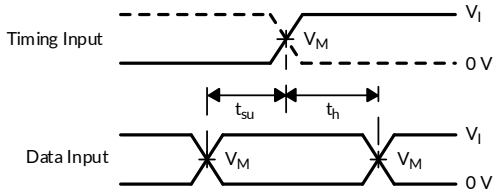
V_{CC}	INPUTS V_I	INPUTS t_r/t_f	V_M	V_{LOAD}	C_L		R_L		V_Δ
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	15pF	30pF	1MΩ	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	15pF	50pF	1MΩ	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	15pF	50pF	1MΩ	500Ω	0.3V



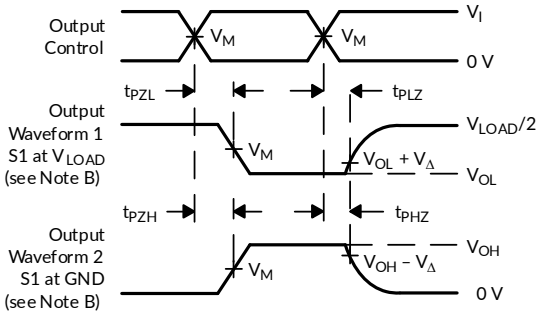
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

DETAILED DESCRIPTION

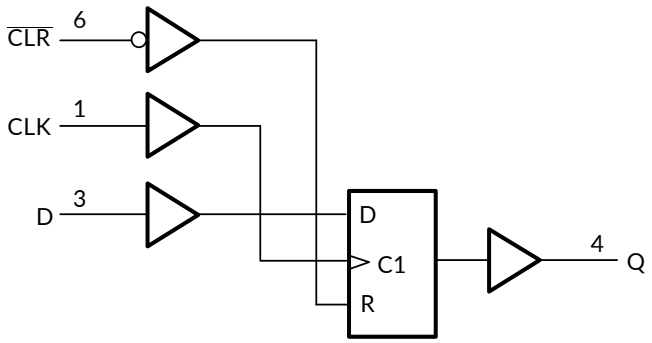
Overview

This single D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G175 device has an asynchronous clear ($\overline{CLR}$) input. When $\overline{CLR}$ is high, data from the input pin (D) is transferred to the output pin (Q) on the clock's (CLK) rising edge. When $\overline{CLR}$ is low, Q is forced into the low state, regardless of the clock edge or data on D.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



Feature Description

The SN74LVC1G175 device has a wide operating V_{CC} range of 1.65 V to 5.5 V, which allows it to be used in a broad range of systems. The 5.5V I/Os allow down translation and also allow voltages at the inputs when V_{CC} = 0.

APPLICATION AND IMPLEMENTATION

Application Information

Multiple SN74LVC1G175 devices can be used in tandem to create a shift register of arbitrary length. In this example, we use four SN74LVC1G175 devices to form a 4-bit serial shift register. By connecting all CLK inputs to a common clock pulse and tying each output of one device to the next, we can store and load 4-bit values on demand. We demonstrate loading the 4-bit value 1101 into memory by setting Serial Input Data to each desired memory bit, and by sending a clock pulse for each bit, we sequentially move all stored bits from left to right (A → B → C → D)

Typical Application

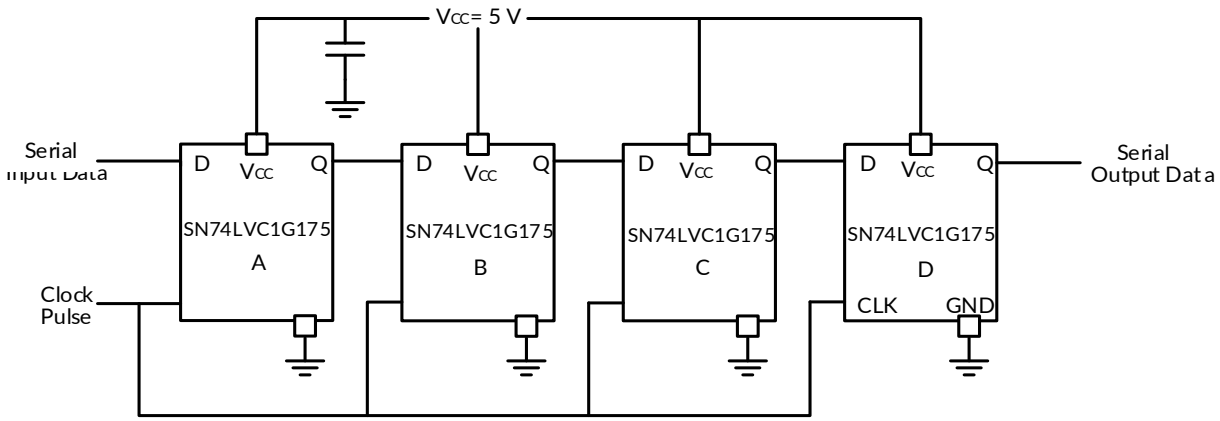


Figure 3. 4-Bit Serial Shift Register

Table 1. Stored Data Values

Serial Input Data	Stored A	Stored B	Stored C	Stored D
1	0	0	0	0
0	1	0	0	0
1	0	1	0	0
1	1	0	1	0
0	1	1	0	1

Design Requirements

The SN74LVC1G175 device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The SN74LVC1G175 allows storing digital signals with a digital control signal. All input signals should remain as close as possible to either 0 V or V_{CC} for optimal operation.

POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF capacitor is recommended and if there are multiple V_{CC} terminals then 0.01µF or 0.022µF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 4 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/O_S so they also cannot float when disabled.

Layout Example

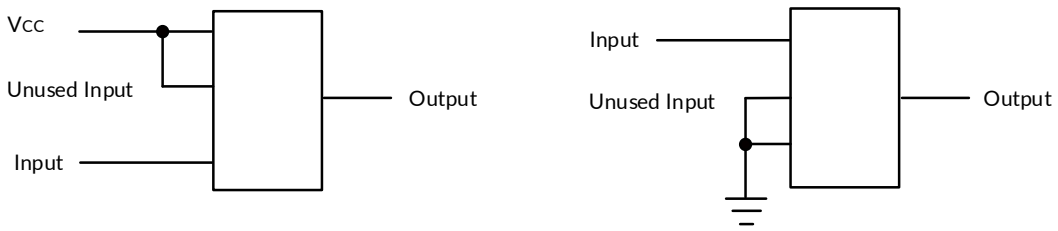
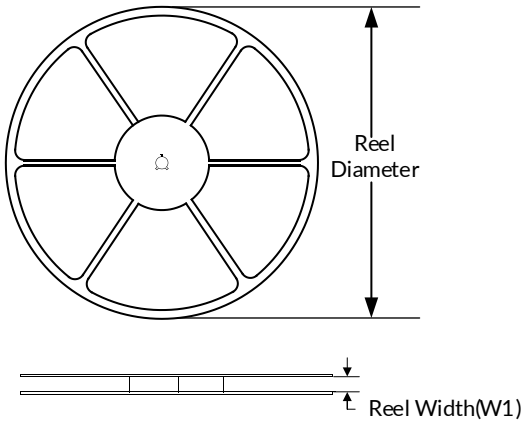


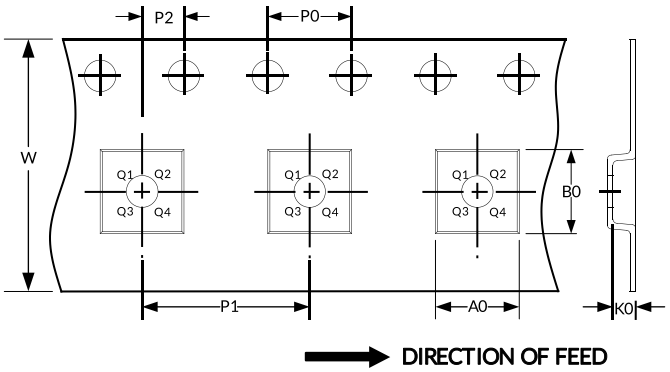
Figure 4. Layout Diagram

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-6	7”	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT23-6	7”	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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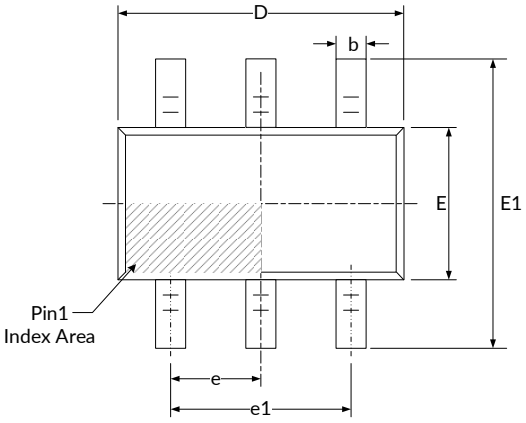
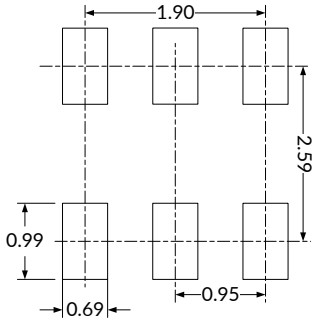
PACKAGE OUTLINE DIMENSIONS

NOTE:

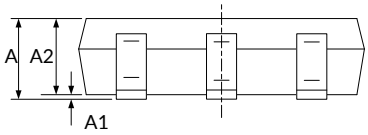
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

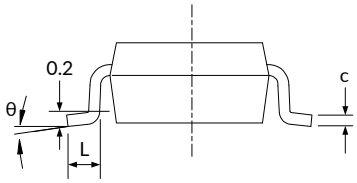
SOT23-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



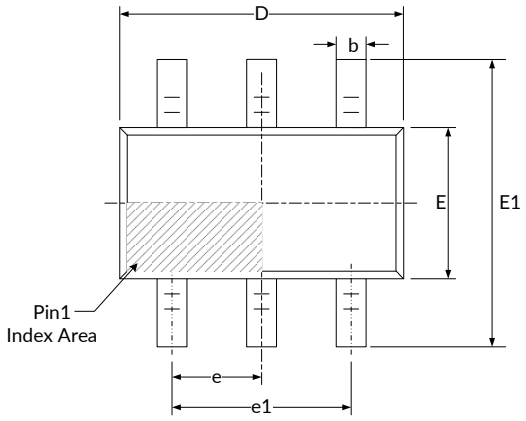


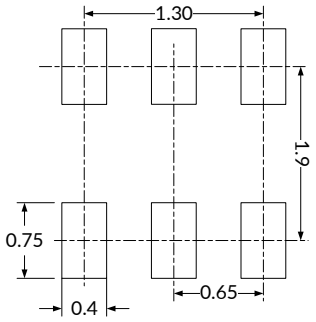
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

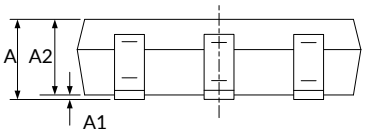
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

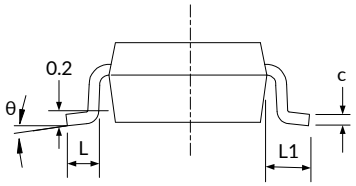
SC70-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D (1)	2.000	2.200	0.079	0.087
E (1)	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(BSC) (2)		0.026(BSC) (2)	
e1	1.300(BSC) (2)		0.051(BSC) (2)	
L	0.260	0.460	0.010	0.018
L1	0.525		0.021	
θ	0°	8°	0°	8°